# N91-21199

# A SOLID-STATE CONTROLLABLE POWER SUPPLY for a MAGNETIC SUSPENSION WIND TUNNEL

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#### **Abstract**

The NASA Langley 6-Inch Magnetic Suspension and Balance System (6-in. MSBS) requires an independently controlled bidirectional dc power source for each of six positioning electromagnets. These electromagnets provide five-degree-of-freedom control over a suspended aerodynamic test model. Existing power equipment, which employs resistancecoupled thyratron-controlled rectifiers as well as ac to de motor-generator converters, is obsolete, inefficient, and unreliable. A replacement six-phase bidirectional controlled bridge rectifier is proposed, which employs power MOSFET switches sequenced by hybrid analog/digital circuits. Full-load efficiency is 80 percent compared with 25 percent for the resistance-coupled thyratron system. Current feedback provides high control linearity, adjustable current limiting, and current overload protection. A quenching circuit suppresses inductive voltage impulses.

It is shown that 20-kHz interference from positioning magnet power into MSBS electromagnetic model position sensors results predominantly from capacitively coupled electric fields. Hence, proper shielding and grounding techniques are necessary. Inductively coupled magnetic interference is negligible.

#### Introduction

The NASA Langley 6-Inch Magnetic Suspension and Balance System (6-in. MSBS) employs six positioning electromagnets to provide five-degree-offreedom control over a suspended aerodynamic test model. Each positioning electromagnet requires up to +90/-30 A dc, supplied by an independent linearly controllable power source. Three of the original power supplies, as shown in figure 1, are thyratroncontrolled rectifier bridges providing a variable voltage up to +250 V (at up to 96 A dc). Each bridge output couples through a resistive T-network to the load and is opposed by a -30 V to -120 V (at up to 1000 A dc) regulated supply. The system is thus capable of providing a variable load voltage between -120 V to +220 V. The resistors, which are water cooled, dissipate excessive wasted energy and have a high failure rate as well. Full-load efficiency of the resistor coupling network is less than 25 percent.

Two of the positioning coils are powered by voltage-controlled ac to dc motor-generator converters (also shown in fig. 1). The remaining coil is powered by a fixed -90 V dc regulated supply. All the existing power equipment is obsolete, bulky, and difficult to maintain because of frequent failures and scarcity of spare parts.

This paper proposes a six-phase 60-Hz bidirectional controlled bridge rectifier employing power MOSFET switches to replace the existing power supply equipment. Elimination of the resistive T-networks increases full-load efficiency to over 80 percent. Bridge switching control pulses are generated by hybrid analog/digital circuitry. A current feedback system provides high control linearity and zero steady state control error (type 1 control).

# **Symbols**

J	
A,B,C	three-phase supply voltages
-A, -B, -C	negative supply voltages
$A_C, B_C, C_C, \\ -A_C, -B_C, -C_C$	cyclic control register bits
$A_I(n)$	odd part of nth current harmonic
$A_p, B_p, C_p \ -A_p, -B_p, -C_p$	phase voltages shifted 30°
$A_V(n)$	odd part of $n$ th voltage harmonic
$A_{xn}, B_{xn}, C_{xn}, \\ -A_{xn}, -B_{xn}, -C_{xn}$	negative comparison pulses
$A_{xp}, B_{xp}, C_{xp}, \ -A_{xp}, -B_{xp}, -C_{xp}$	positive comparison pulses
$B_I(n)$	even part of $n$ th current harmonic
$B_V(n)$	even part of nth voltage harmonic
BW	bandwidth
DII	Danuwidin
$C_I(n)$	nth current harmonic
$C_I(n)$	nth current harmonic
$C_I(n)$ $C_{OA}, C_{OB}, C_{PA}, C_{PB}$	nth current harmonic fault detection comparators
$C_{I}(n)$ $C_{OA}, C_{OB}, C_{PA}, C_{PB}$ $C_{V}$	nth current harmonic fault detection comparators fault protection capacitor
$C_{I}(n)$ $C_{OA}, C_{OB}, C_{PA}, C_{PB}$ $C_{V}$ $C_{V}(n)$	nth current harmonic fault detection comparators fault protection capacitor nth voltage harmonic
$C_I(n)$ $C_{OA}, C_{OB}, C_{PA}, C_{PB}$ $C_V$ $C_V(n)$ $D_1, \dots, D_6$	nth current harmonic fault detection comparators fault protection capacitor nth voltage harmonic gated firing pulse current control command
$C_I(n)$ $C_{OA}, C_{OB}, C_{PA}, C_{PB}$ $C_V$ $C_V(n)$ $D_1, \dots, D_6$ $E_I$	nth current harmonic fault detection comparators fault protection capacitor nth voltage harmonic gated firing pulse current control command voltage absolute peak of phase
$C_I(n)$ $C_{OA}, C_{OB}, C_{PA}, C_{PB}$ $C_V$ $C_V(n)$ $D_1, \dots, D_6$ $E_I$	nth current harmonic fault detection comparators fault protection capacitor nth voltage harmonic gated firing pulse current control command voltage absolute peak of phase voltage electromagnetic position
$C_I(n)$ $C_{OA}, C_{OB}, C_{PA}, C_{PB}$ $C_V$ $C_V(n)$ $D_1, \dots, D_6$ $E_I$ $E_M$ EPS	nth current harmonic fault detection comparators fault protection capacitor nth voltage harmonic gated firing pulse current control command voltage absolute peak of phase voltage electromagnetic position sensor
$C_I(n)$ $C_{OA}, C_{OB}, C_{PA}, C_{PB}$ $C_V$ $C_V(n)$ $D_1, \dots, D_6$ $E_I$ $E_M$ $EPS$ $e(t)$ $G_A, G_B, G_C$	nth current harmonic fault detection comparators fault protection capacitor nth voltage harmonic gated firing pulse current control command voltage absolute peak of phase voltage electromagnetic position sensor time varying phase voltage sequential phase firing

$\dot{\imath}$	instantaneous load current
$i_0$	steady state load current at $x = 0$
i(x)	steady state load current at angular time $x$
K	linear gain constant
L	load inductance, H
MOSFET	metal-oxide-semiconductor field effect transistor
MSBS	magnetic suspension and balance system
N	440-V neutral
n	Fourier series coefficient index
PI	proportional plus integral
$Q_F$	set bit for quenching thyristor
$R, R_L$	load resistance
$R_C$	fault-limiting resistance
$R_Q$	quenching resistance
rms	root mean square
$S_x$	sign of input command voltage
s	Laplace transform variable
T	time duration of periodic waveform, sec
$T_Q$	quenching thyristor
t	time
$V_{ m bias}$	bias voltage
$V_R$	average load voltage
$V_{R,\max}$	maximum attainable absolute load voltage
$\boldsymbol{x}$	angular time, radians
y(t)	T-second averaging integrator output
$\theta$	phase angle, radians
$ au_D$	dominant closed loop time constant
$\phi$	MOSFET firing angle,

radians

$\phi_R$	firing angle required for average load voltage $V_R$ , radians
$\omega$	frequency, radians/sec
$\omega_0,\omega_1$	break frequencies, radians/sec

### **Design Description**

# Six-Phase Power Source

Three-phase 440-V power is stepped down via either a 440-V wye to a 63.5-V six-phase star (as shown in fig. 2) which can furnish 85.3 average dc volts, or via a 440-V three-phase delta to a 110-V six-phase star (not shown) which can furnish 148 dc volts. The resistance of each positioning magnet coil determines the required power supply voltage range.

# Voltage-Controlled Bridge Rectifier

Bidirectional conduction in each leg of the sixphase bridge rectifier is controlled by two power-MOSFET switches connected in parallel with opposing polarities, as illustrated in figures 3 and 4. Note that each MOSFET is protected by a series reverse-blocking diode. This bidirectional design allows load voltage to be controlled entirely by varying the switching times at each leg. Hybrid analog/digital circuitry determines sequential switching times at successive bridge legs necessary to produce dc load voltage proportional to the control voltage. Load inductance provides natural current smoothing. In case of bridge current interruption, a quenching circuit shunts load current to ground to prevent inductive voltage impulses.

All MOSFET gates are optically isolated from control circuits. Isolation is necessary because none of the bridge MOSFET source terminals can be grounded; all source terminals must connect either to the load or to a phase voltage leg. Refer to figure 4 for bridge leg details. Isolation also protects 5-V control logic from ac power circuits. Gate voltage is supplied to the MOSFET through an opto-isolator from a floating dc power supply which adds a fixed de bias to the bridge leg voltage. To drive the active MOSFET into saturation, each bridge leg requires an independent bias supply. During cutoff a bleeder resistor from gate to source drains off gate charge, which accumulates because of opto-coupler off-state leakage. A blocking diode in series with the floating bias supply is provided to prevent reverse conduction through the opto-coupler.

#### **Timing Control Circuit**

Figure 5 illustrates the six-phase voltage waveforms labeled A, -C, B, -A, C, and -B referred to as phase voltages. Angular time  $\omega t$  (also denoted by x) is expressed in radians relative to the positive zero crossing of phase A voltage. Note that in figures 5 and 8, a corresponding time axis is used. Switch-off time is coincident with the switch-on time of the succeeding phase. At steady state, each bridge leg conducts for a  $\pi/3$ -radian duration.

The relation between firing time in radians, hereafter denoted firing angle  $\phi$ , and control voltage  $E_I$  required for linear control of de load voltage is now derived. For algebraic convenience let time t equal zero when phase voltage e(t) turns on. Thus

$$e(t) = E_M \sin(\omega t + \phi) \tag{1}$$

where

$$\pi/3 \le \phi \le 5\pi/6$$

and  $\omega t$  ranges from 0 to  $\pi/3$ . Load current i is described by

$$di/dt + Ri/L = (E_M/L)\sin(\omega t + \phi) \tag{2}$$

where L is the load inductance and R is the series load resistance. The solution to equation (2) is

$$i(x) = i_0 e^{-Rx/\omega L} - \left[ E_M / \sqrt{R^2 + (\omega L)^2} \right] \left[ \sin(\phi - \theta) e^{-Rx/\omega L} - \sin(x + \phi - \theta) \right]$$
 (3)

where  $x = \omega t$ 

$$\theta = \tan^{-1}(\omega L/R)$$

$$i_0 = i(0)$$

$$\omega = 120\pi$$

During steady state operation, x passes from 0 to  $\pi/3$  radians. Because the load is inductive, i(x) will be continuous at switching points. Therefore

$$i_0 = i(\pi/3) \tag{4}$$

Solving equations (3) and (4) for  $i_0$  yields

$$i_{0} = \frac{E_{M} \left[ \sin(\pi/3 + \phi - \theta) - e^{-\pi R/3\omega L} \sin(\phi - \theta) \right]}{\left( 1 - e^{-\pi R/3\omega L} \right) \sqrt{R^{2} + (\omega L)^{2}}}$$
(5)

Combine equations (5) and (3) to obtain steady state load current as a function of angular time x; thus

$$i(x) = \frac{E_M \left[ \cos(\phi - \theta + \pi/6)e^{-Rx/\omega L} / (1 - e^{-\pi R/3\omega L}) + \sin(x + \phi - \theta) \right]}{\sqrt{R^2 + (\omega L)^2}}$$
(6)

where  $0 \le x \le \pi/3$ .

Average steady state load current is obtained by integrating equation (6) over the  $\pi/3$ -radian conduction interval to give

$$I_{\rm av}(\phi) = [3E_M/(\pi R)]\sin(\phi + \pi/6)$$
 (7)

where  $\pi/3 \le \phi \le 5\pi/6$ .

Firing angle  $\phi_R$  required to produce average load voltage  $V_R$  is determined electronically as shown in figures 6(a) and 6(b). This analog circuit solves equation (7) for  $\phi_R$ , given  $V_R$ , as

$$\phi_R = \sin^{-1}(\pi V_R/3E_M) - \pi/6 \tag{8}$$

and  $V_{R,\text{max}} = 3E_M/\pi$  is the maximum available average dc load voltage.

Lead circuits shift the six phase voltages  $\pi/6$  radian. These shifted voltages, labeled  $A_p, \ldots, -B_p$ , are compared with  $V_R$ , producing comparison pulses  $A_{xp}, \ldots, -B_{xp}$  for positive  $V_R$  and  $A_{xn}, \ldots, -B_{xn}$  for negative  $V_R$ . The rising edge of each comparison pulse occurs at the proper firing angle  $\phi_R$  for the corresponding phase voltage.

The comparator and logic circuit shown in figure 7 generates six sequential pulses, labeled  $G_A, \ldots, G_{B-}$ , beginning at  $\pi/3$ -radian intervals. Each pulse has a  $\pi/2$ -radian duration and defines the  $\pi/3$ - to  $5\pi/6$ -radian firing window during which the corresponding phase may turn on, as shown in figure 8. Pulses  $G_A, \ldots, G_{B-}$  are combined with comparison pulses  $A_{xp}, \ldots, -C_{xp}, A_{xn}, \ldots, -C_{xn}$  in the network of figure 9 to produce gated firing pulses  $D_1, \ldots, D_6$ . This circuit selects the proper comparison pulse, depending on the polarity of  $V_R$ , and blocks spurious impulses outside the  $\pi/3$  to  $5\pi/6$ firing window for each phase. Pulses  $D_1, \ldots, D_6$ sequentially set gating bits  $A_C, \ldots, -B_C$  in the six-bit cyclic register illustrated in figure 10. Register bits  $A_C$  through  $-B_C$  drive the corresponding opto-couplers, which in turn drive the corresponding MOSFET gates.

The protective logic network, shown in figure 10, resets the previously active register bit. Table I lists, for each active bit, the allowable bits which may be set by the next gated firing pulse (possible next bit), and also previously active bits reset by the protective gating network (bits which active bit turns off). This design assures that at most only one bit of the six is set (only one bridge leg is active), which prevents phase-to-phase short circuits. Furthermore, all bits are reset if an error condition is detected, which opens all legs of the bridge and closes both quenching switches.

Figures 11 through 16 illustrate simulated transient responses of bridge output voltage and load current (without current feedback) to step and ramp control inputs for an L/R time constant of 0.012 sec. Responses to step inputs of 100 percent, 50 percent, and -20 percent of full load appear in figures 11 through 13. Output voltage centers about the control input within 1/360 sec. Load current response is nearly exponential with an additive 360-Hz ripple.

Figures 14 and 15 illustrate current and voltage responses to a ramp input with a slope of 100 percent of and -100 percent of full scale in 20 msec, which is equal to the maximum slope of an 8-Hz sine wave. Note that the sawtooth-shaped load voltage is well-centered about the control input ramp voltage. However, load current lags the control voltage. Although initially zero, current lag increases to the normal constant lag of a first-order ramp response. Response to a ramp control input with a slope of 200 percent of full scale in 20 msec appears in figure 16. Output voltage is no longer symmetric about the control input voltage. Load current, initially zero, attempts to follow the input with first-order lag.

The switching control logic will maintain sequential switching synchronism despite discontinuous or rapidly changing control voltage. Additional simulation studies verify that the switching control circuits function correctly for high-frequency control voltage disturbances.

Table I. State Transition Table for Cyclic Control Register

	Bits which	Bits which	
Active	turn off	active bit	Possible
bit	active bit	turns off	next bit
A	-C, C, -A	B, -B, -A	-C,C
-C	B, -B, C	A, -A, C	-B,B
B	-A, A, -B	C, -C, -B	-A, A
-A	C, -C, A	-B, B, A	-C,C
C	-B, B, -C	A, -A, -C	-B,B
-B	A, -A, B	-C, C, B	-A, A

#### **Current Feedback Circuit**

Current feedback provides four improvements to power source performance:

- 1. Adjustable dc current limiting
- 2. dc current overload protection
- 3. Improved linearity between control input voltage and average dc output
- 4. Zero steady state control error

Current limiting and feedback circuitry appears in figure 17. The current limiting feature provides an adjustable bound on average load current magnitude, which also prevents current overload. The nonlinear saturation block in the figure employs clamping diodes which restrict input control voltage magnitude  $|E_I|$  to an adjustable reference voltage. This, in turn, limits the command voltage at the summing input of the current feedback circuit.

Load current is sensed by a bidirectional Hall-effect current transducer followed by a 30-Hz low-pass filter. The error voltage, conditioned by a proportional plus integral compensator, drives the bridge firing control input.

Table II. Positioning Coil Constants

Coil	Load resistance $R, \Omega$	Load inductance L, H	Coil BW, Hz	Time constant L/R, sec
Axial	2.0	0.36	0.88	0.18
Inner saddle	.5	.008	9.9	.016
Outer saddle	.9	.016	9.0	.018
Drag	2.0	.016	19.9	.008
Side and lift	1.0	.40	.40	.40

Resistance and inductance of the positioning coils limit open-loop bandwidths of the positioning circuits, as listed in table II. The current feedback control loop is modeled in figure 18 as a first-order linear plant, PI compensator, and low-pass filter. With a single-pole filter, the open-loop transfer function is

$$H_0(s) = (K/R)(1 + s/\omega_1)/[s(1 + Ls/R)(1 + s/\omega_0)]$$
(9)

Root locus analysis is employed to determine the best loop gain K/R for each of the positioning coils listed in table II. Figure 19 illustrates the root locus plot (ref. 1) of equation (9) for the axial coil circuit, with time constant L/R=0.16 sec and break frequencies  $\omega_0=60\pi$  radians/sec and  $\omega_1=20\pi$  radians/sec. It can be seen in figure 19 that the fastest closed-loop time response with acceptable damped oscillation occurs for a loop gain of K/R of 1500. providing a closed-loop time constant of 0.0189 sec and a damping coefficient of 0.375. Although practical loop gain K/R is limited by amplifier and rectifier bridge saturation, as well as noise sensitivity, the circuit is unlikely to saturate for error voltages less than 0.5 V for K/R=1500.

Figure 20 illustrates the root locus plot for the inner saddle coil (L/R=0.016 sec), with break frequencies  $\omega_0$  and  $\omega_1$  unchanged. For these constants, the dominant closed-loop time constant  $\tau_D$  can be decreased only to a minimum of 0.0113 sec at a loop gain of 47.5. Note that loop gains greater than 47.5 merely produce unwanted damped oscillation with no improvement in time response.

Similar root locus analyses are required to determine closed-loop gains for the remaining positioning coil control circuits.

#### **Fault Protection Circuits**

Although the current feedback system limits average dc load current, instantaneous bridge leg current

can exceed safe magnitudes and durations if a load short circuit occurs. In addition, an open-circuit failure in a conducting bridge leg will produce a sharp inductive overvoltage impulse across the other non-conducting bridge legs. Both fault conditions can destroy bridge leg semiconductors. Overvoltage and overcurrent detecting circuits are provided to quickly turn off the bridge and to shunt inductive load current to ground in case of a fault.

The load overvoltage fault protection circuit is shown in figure 21. If supply current is interrupted, capacitor  $C_V$ , which is connected in parallel with load L, accumulates load current. As soon as the increasing inductive load voltage exceeds the fault threshold level detected by comparators  $C_{PA}$  and  $C_{PB}$ , bit  $Q_F$  is set. This bit, in turn, fires quenching thyristor  $T_Q$ , which shunts load current through resistor  $R_Q$  to ground. Figures 22 and 23 illustrate a worst case load voltage inductive impulse and quenching transient following a source current interruption. (Fig. 22 shows the initial 100  $\mu$ sec of the fault.)

Capacitor  $C_V$  is sized to limit increasing inductive load voltage to a safe level before thyristor  $T_Q$  fires. This capacitor adds an open-loop time constant of  $C_V(R_C+R_L)$ , which is too small  $(1\times 10^{-5})$  to affect the previous root locus analysis. Likewise, resistor  $R_Q$  is chosen low enough to safely limit load voltage during inductor current quenching. The decay time constant is  $L/(R_L+R_Q)$ .

The current overload detection circuit of figure 24 is activated when the load inductor becomes shorted. Instantaneous load current is averaged by a T/2-sec delay two-pole Bessel filter, which closely approximates a T-sec averaging integrator of the form

$$y(t) = 1/T \int_{t-T}^{t} i(t) dt$$
 (10)

Averaging eliminates load current transient impulses of short duration. Delay T/2 is chosen sufficiently small to protect bridge leg semiconductors from short-circuit current damage. Whenever a current overload is sensed, the bridge is disabled, and quenching thyristor  $T_Q$  fires.

A short circuit is more likely to occur in a bridge leg semiconductor than in a positioning coil. Internal bridge short circuit protection circuitry would have to be replicated in each of the six bridge legs. Since the expense of internal short circuit protection circuits would exceed the cost of replacement bridge semiconductors, protection against short circuits internal to the bridge itself is provided by power transformer circuit breakers and fuses only.

# Harmonic Analysis of Rectified Load Voltage and Current

The 6-in. MSBS is equipped with an electromagnetic position sensing system (EPS) which employs a set of five sensor coil pairs wound on a cylindrical cage installed in the test section. An amplitude-modulated 20 kHz sinusoidal carrier inductively couples into the EPS sensor coils. Interference from positioning magnet power harmonics near 20 kHz can interfere with EPS operation. Fourier series analysis of positioning magnet voltage and current waveforms at steady state allows computation of their harmonic amplitudes.

As the firing angle varies from  $\pi/3$  to  $5\pi/6$  radians, load voltage becomes increasingly discontinuous, thus increasing the ratio of each voltage harmonic to the maximum dc voltage level at  $\phi = \pi/3$ . Since the inductance of the positioning coil forces load current to be continuous, the ratios of current harmonic amplitudes to maximum dc current are significantly less than the corresponding voltage harmonic ratios. The Fourier series coefficient equations for load voltage and current, as functions of firing angle, are derived in the appendix.

Table III lists rms levels of the 55th and 56th voltage and current harmonics (19.80 and 20.16 kHz) in dB, relative to full-load average dc level for firing angles ranging from  $\pi/3$  to  $5\pi/6$  radians in  $\pi/12$  radian increments. Circuit constants are  $R/\omega L=0.1,\ R=1\Omega,\ {\rm and}\ \omega=120\pi.$ 

Table III. The rms Load Voltage and Current Harmonic Levels Relative to Full-Load dc

		55th harmonic 19.80 kHz		56th harmonic 20.16 kHz	
Firing Percent angle, of full radians load do	Voltage, dB	Current,	Voltage,	Current,	
$\pi/3$	100	- 98.1	-117.4	98.4	-117.7
$5\pi/12$	96.6	59.5	116.0	59.6	116.3
$\pi/2$	86.6	53.8	115.3	53.9	-115.6
$7\pi/12$	70.7	50.8	115-2	50.9	-115.5
$2\pi/3$	50.0	~49.0	-115.7	49.2	115.0
$3\pi/4$	25.9	-48.0	-117.0	48.2	-1173
$5\pi/6$	0	-47.8	119.1	47.9	-119.4

Note that current harmonic amplitudes vary only slightly with firing angle  $\phi$ , whereas voltage harmonic amplitudes increase markedly with  $\phi$ . Moreover, relative voltage harmonic amplitudes are 60 to 70 dB greater than corresponding relative current harmonic amplitudes for  $\phi$  greater than  $\pi/3$  radians.

Since voltage harmonics predominate and current harmonic amplitudes are more than 115 dB below the maximum de level, only capacitively coupled interference from positioning magnet voltage into EPS sensor coils is significant at 20 kHz. Thus, appropriate grounding and shielding measures are necessary to minimize positioning system interference into the EPS system. Although inductively coupled interference is low, the 6-in. MSBS is equipped with a Faraday shield installed around the EPS coil cage to attenuate inductive coupling from positioning circuits.

# **Concluding Remarks**

This paper has proposed a solid state voltage-controlled power source to drive positioning magnets in a magnetic suspension and balance system. The design employs a six-phase bidirectional bridge switched by power MOSFET switches controlled, in turn, by hybrid analog/digital sequential switching circuitry. Load voltage level and polarity are entirely determined by switching times at each bridge leg, such that dc load voltage is proportional to input control voltage. Control circuits are optically isolated from power circuits. An automatic quenching circuit shunts load current to ground if bridge current is interrupted.

Positioning coil time constants limit open-loop transient response. Current feedback with integral plus proportional compensation provides improved linearity between the control input and dc output along with zero steady-state error and current over-load protection. Integral plus proportional feedback compensation also improves transient decay time in coil currents.

Fourier series analysis of steady state load voltage and current shows that voltage harmonics relative to full-load dc volts predominate over corresponding relative load current harmonics by 60 to 70 dB. Consequently, positioning system power interference into the electromagnetic position sensing system arises primarily from a capacitively coupled electric field. For this reason, proper shielding and grounding procedures are necessary to minimize EPS interference near 20 kHz.

A low voltage prototype of this design has been developed. Laboratory testing and extensive circuit simulation confirm that design criteria have been met.

#### Reference

 Kuo, Benjamin C.: Automatic Control Systems. Prentice Hall, Inc., 1987.

# **Appendix**

# **Obtaining Fourier Series Coefficients**

 $C_I(n) = \left[A_I^2(n) + B_I^2(n)\right]^{1/2}$ 

The Fourier series coefficient  $C_V(n)$  of the nth voltage harmonic is obtained by integrating equation (1) over the period of conduction. Thus

$$A_V(n) = 6E_M/\pi \int_0^{\pi/3} \sin(x+\phi) \sin 6nx \, dx = \left[36E_M n/\pi (36n^2 - 1)\right] \sin(\phi - \pi/3) \tag{A1a}$$

$$B_V(n) = 6E_M/\pi \int_0^{\pi/3} \sin(x+\phi) \cos 6nx \, dx = \left[ 6E_M/\pi (36n^2 - 1) \right] \sin(\phi - \pi/6) \tag{A1b}$$

$$C_V(n) = \left[A_V^2(n) + B_V^2(n)\right]^{1/2}$$
 (A1c)

Similarly, the Fourier series coefficient  $C_I(n)$  of the nth current harmonic is obtained from equation (6) as

$$A_{I}(n) = \left[ 6E_{M}n/\pi\sqrt{R^{2} + (wL)^{2}} \right] \int_{0}^{\pi/3} \left\{ \cos(\phi - \theta + \pi/6) \left[ e^{-Rx/\omega L} / \left( 1 - e^{-\pi R/\omega L} \right) \right] \right.$$

$$\left. + \sin(x + \phi - \theta) \right\} \sin 6nx \, dx$$

$$= 36E_{M}/\pi\sqrt{R^{2} + (wL)^{2}} \left\{ \cos(\phi - \theta + \pi/6) \left[ (R/\omega L)^{2} - 1 \right] / \left[ 36n^{2} + (R/\omega L)^{2} \right] (36n^{2} - 1) \right\} \quad \text{(A2a)}$$

$$B_{I}(n) = \left[ 6E_{M}n/\pi\sqrt{R^{2} + (wL)^{2}} \right] \int_{0}^{\pi/3} \left\{ \cos(\phi - \theta + \pi/6) \left[ e^{-Rx/\omega L} / \left( 1 - e^{-\pi R/\omega L} \right) \right] \right.$$

$$\left. + \sin(x + \phi - \theta) \right\} \cos 6nx \, dx$$

$$= 6E_{M}/\pi\sqrt{R^{2} + (wL)^{2}} \left\{ \left[ \sin(\phi - \theta + 5\pi/6) / (36n^{2} - 1) \right] \right.$$

$$\left. - \left[ \cos(\phi - \theta + \pi/6) / 36n^{2} + (R/\omega L)^{2} \right] \right\} \quad \text{(A2b)}$$

(A2c)

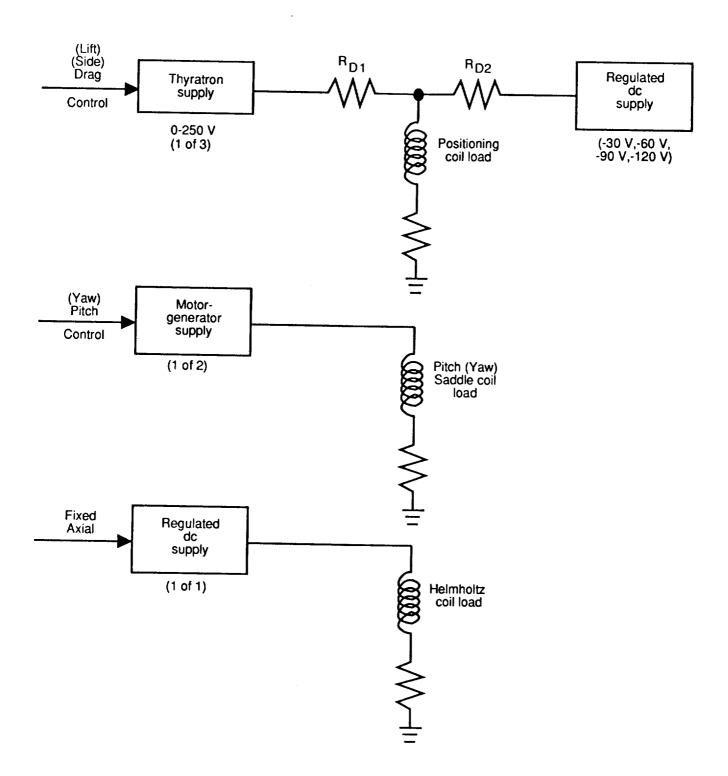


Figure 1. Existing controlled power supply configuration.

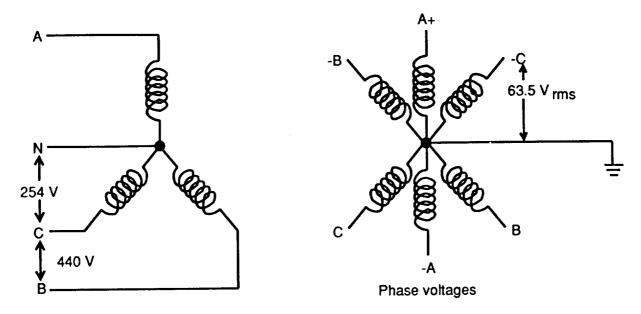


Figure 2. Three-phase wye to six-phase star transformer.

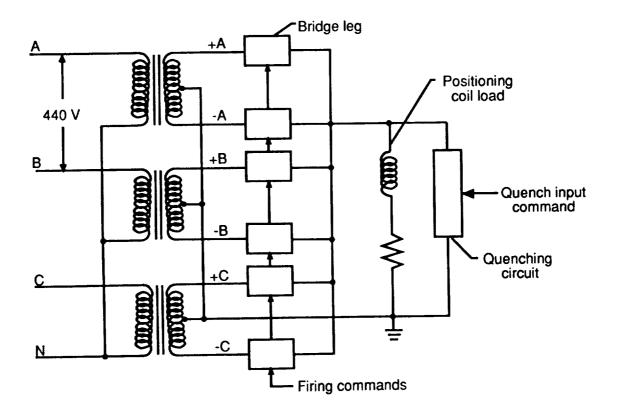


Figure 3. Six-phase bidirectional rectifier bridge with quenching circuit.

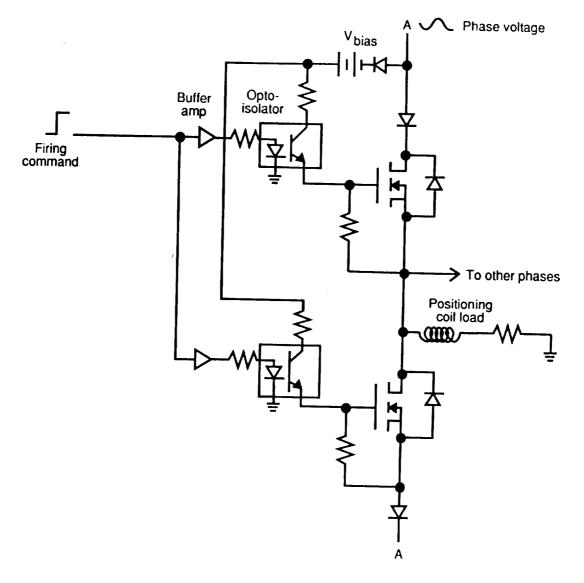


Figure 4. Optical isolation and biasing circuit for phase-A gate circuits.

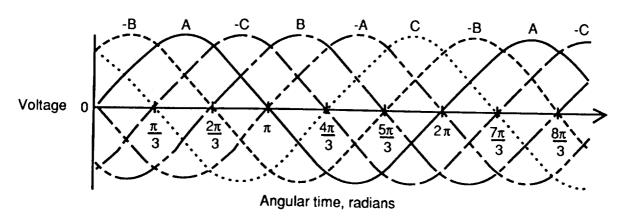
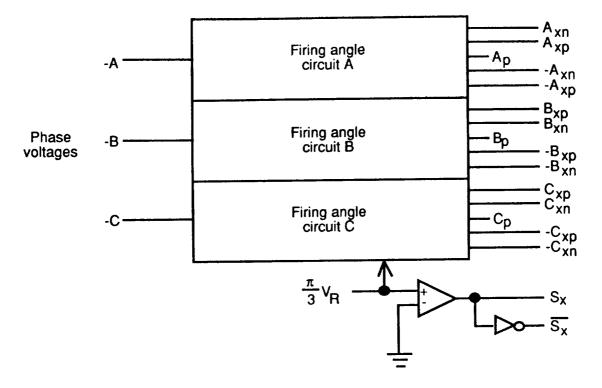
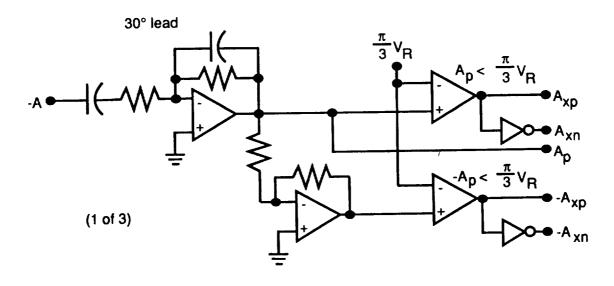


Figure 5. Six-phase sinusoidal voltages.



(a) Circuit block diagram.



(b) Circuit detail.

Figure 6. Determination of firing angle.

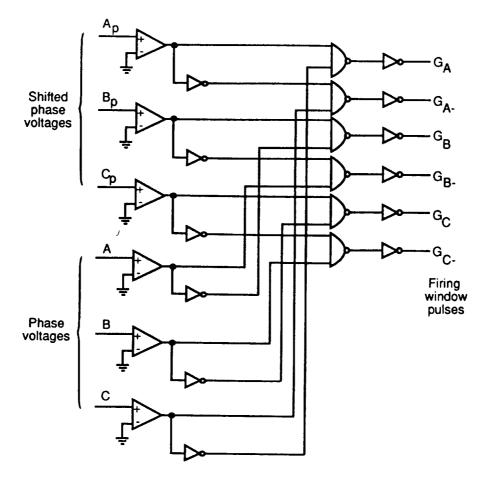


Figure 7. Phase firing window detection logic circuit.

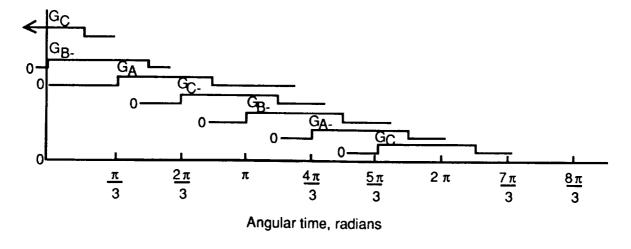


Figure 8. Phase firing windows.

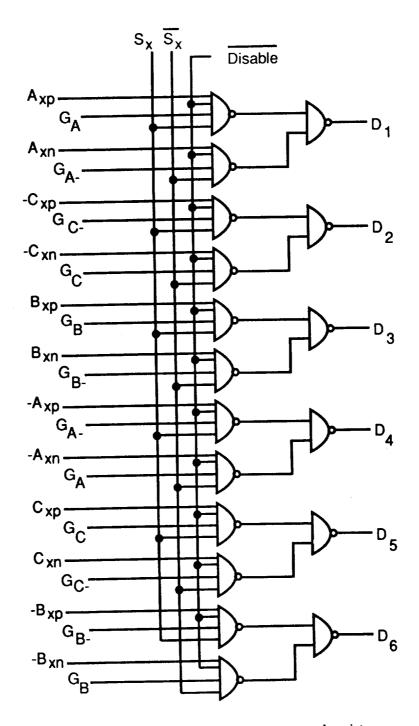


Figure 9. Commutation logic for cyclic control register.

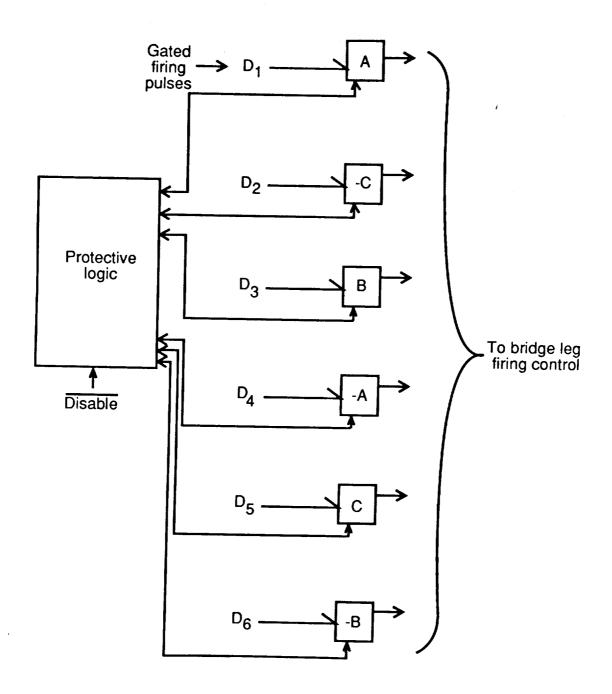


Figure 10. Cyclic control register.

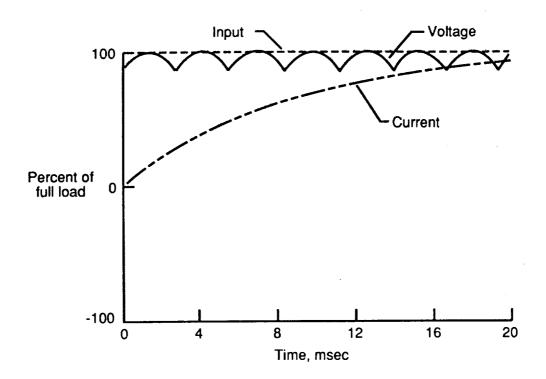


Figure 11. Load voltage and current response to a 100-percent step input.

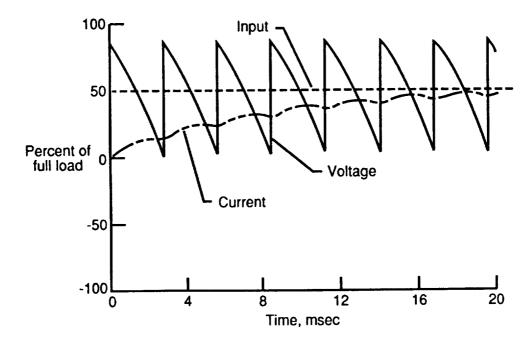


Figure 12. Load voltage and current response to a 50-percent step input.

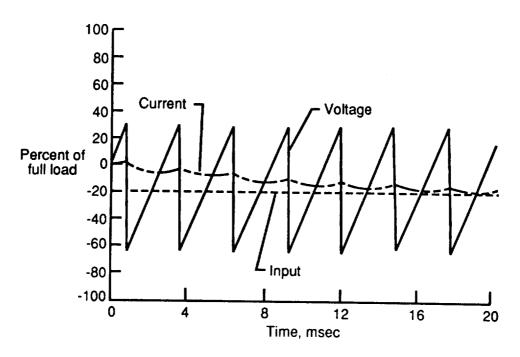


Figure 13. Load voltage and current response to a -20-percent step input.

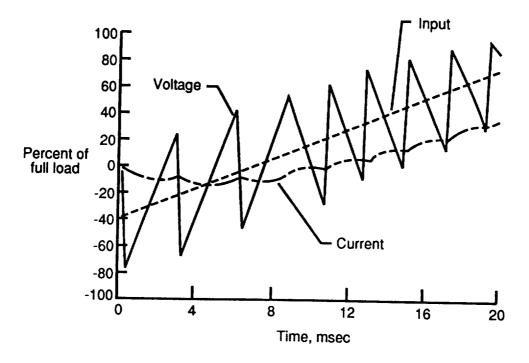


Figure 14. Load voltage and current response to a 100-percent, 20 msec ramp input.

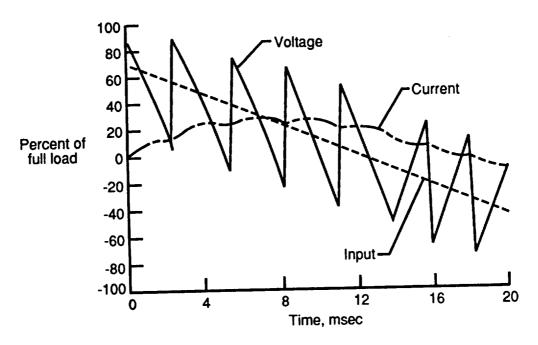


Figure 15. Load voltage and current response to a -100-percent, 20 msec ramp input.

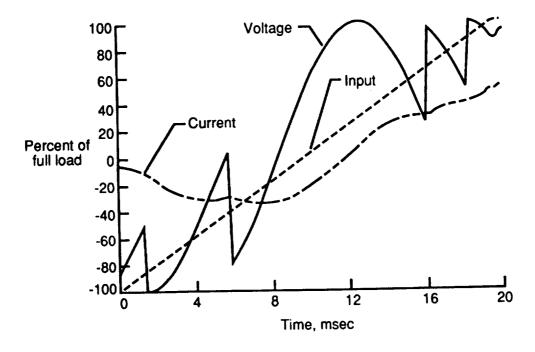


Figure 16. Load voltage and current response to a 200-percent, 20 msec ramp input.

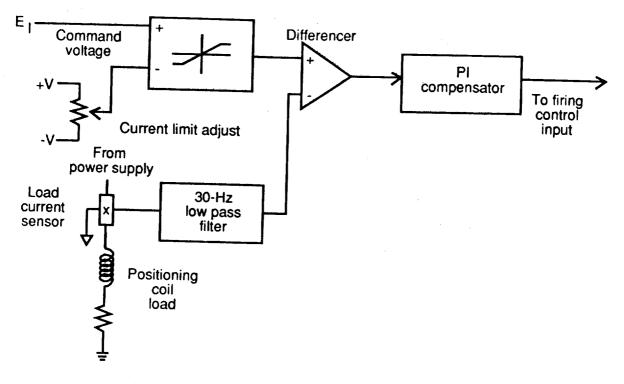


Figure 17. Current limiting and current feedback circuit.

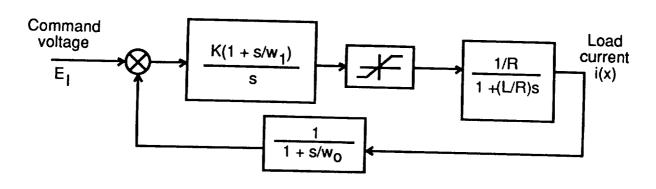


Figure 18. Positioning magnet current feedback control.

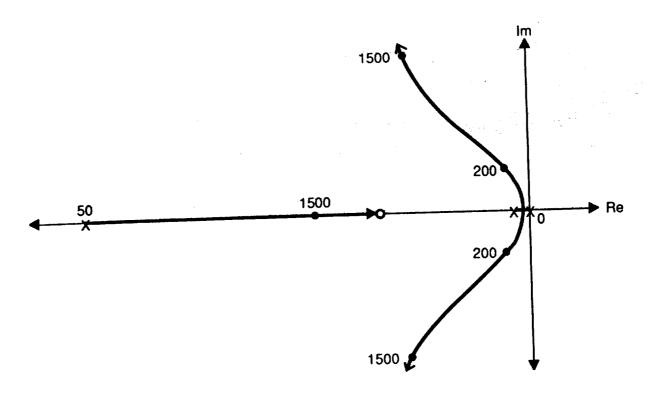


Figure 19. Root locus for PI current feedback control.  $L/R=0.16~{
m sec.}$ 

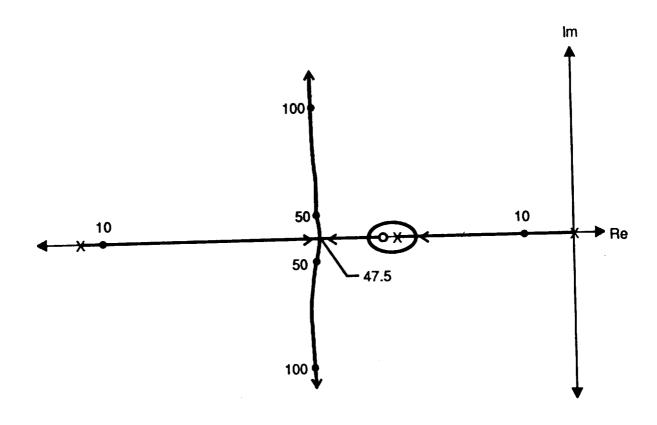


Figure 20. Root locus for PI current feedback control. L/R=0.016 sec.

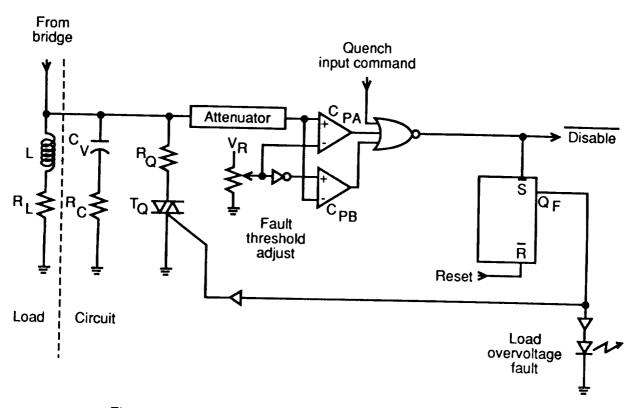


Figure 21. Load overvoltage fault detection and quenching circuit.

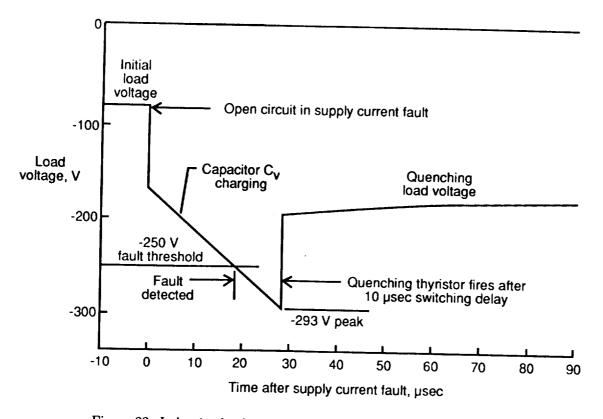


Figure 22. Inductive load voltage impulse after bridge open circuit.

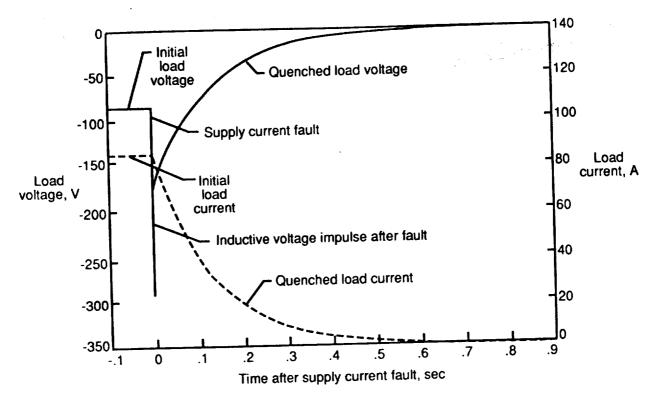


Figure 23. Quenched load voltage and current after bridge open circuit.

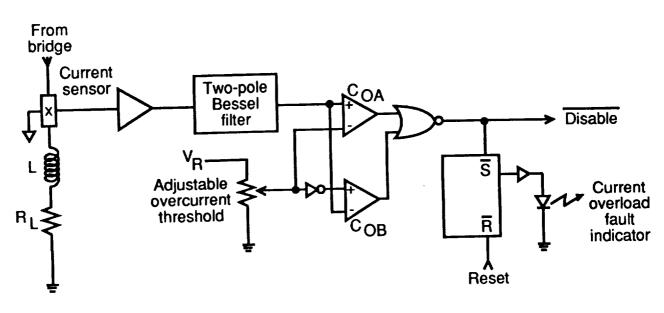


Figure 24. Current overload fault detection circuit.